FIG. 1

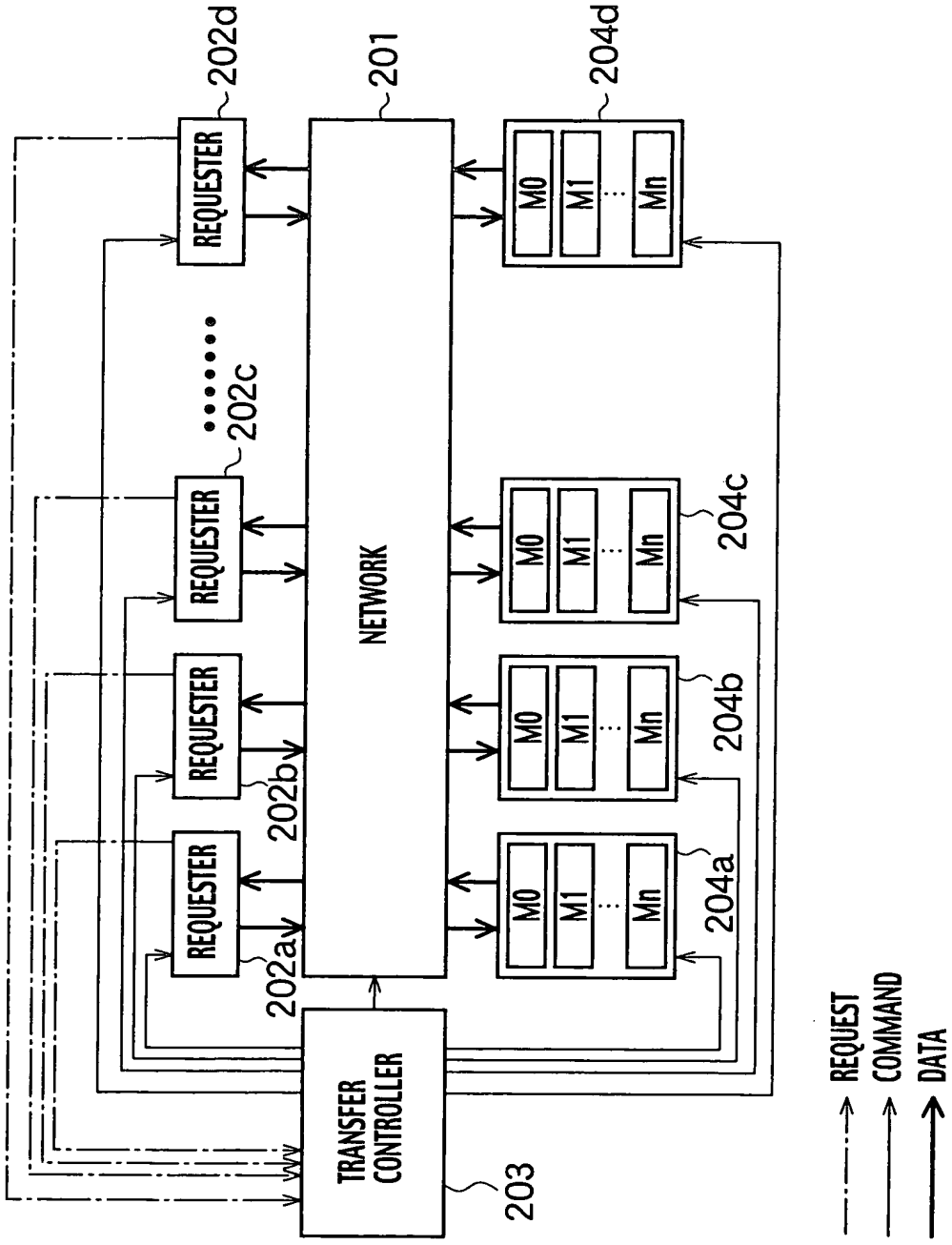

202d
201
204d
REQUESTER
M0
M1
Mn
202c
REQUESTER
NETWORK
M0
M1
Mn
204c
REQUESTER
202b
M0
M1
Mn
204b
REQUESTER
202a
M0
M1
Mn
204a
TRANSFER CONTROLLER
203
REQUEST
COMMAND
DATA

FIG. 2

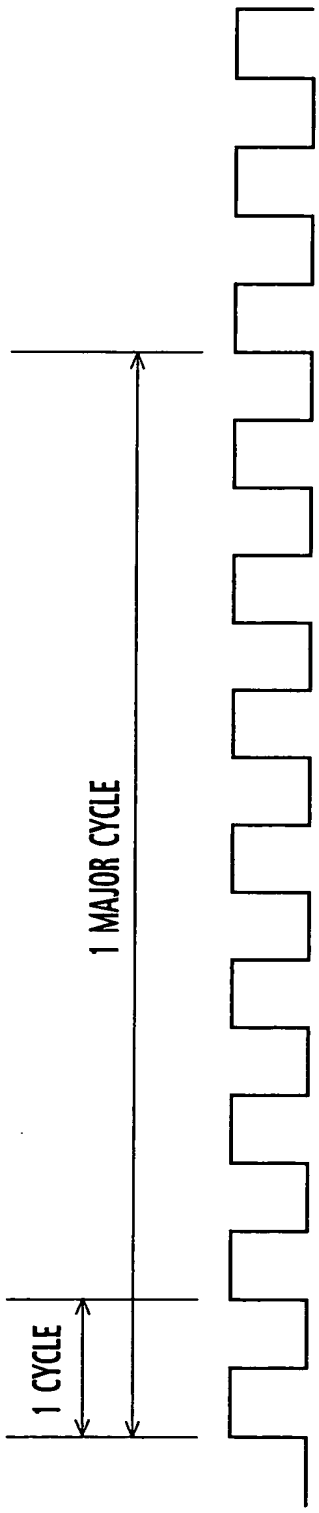


FIG. 3

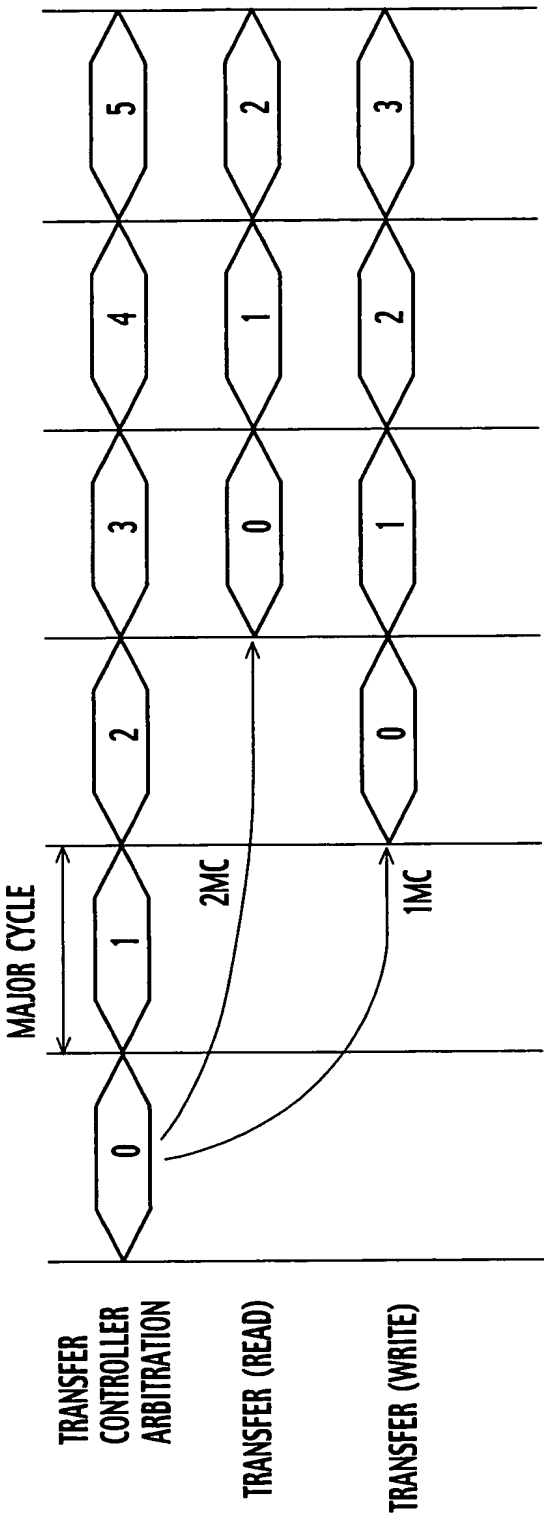

MAJOR CYCLE
2MC
1MC
0
1
2
3
4
5
0
1
2
0
1
2
3
TRANSFER CONTROLLER ARBITRATION
TRANSFER (READ)
TRANSFER (WRITE)

FIG. 4

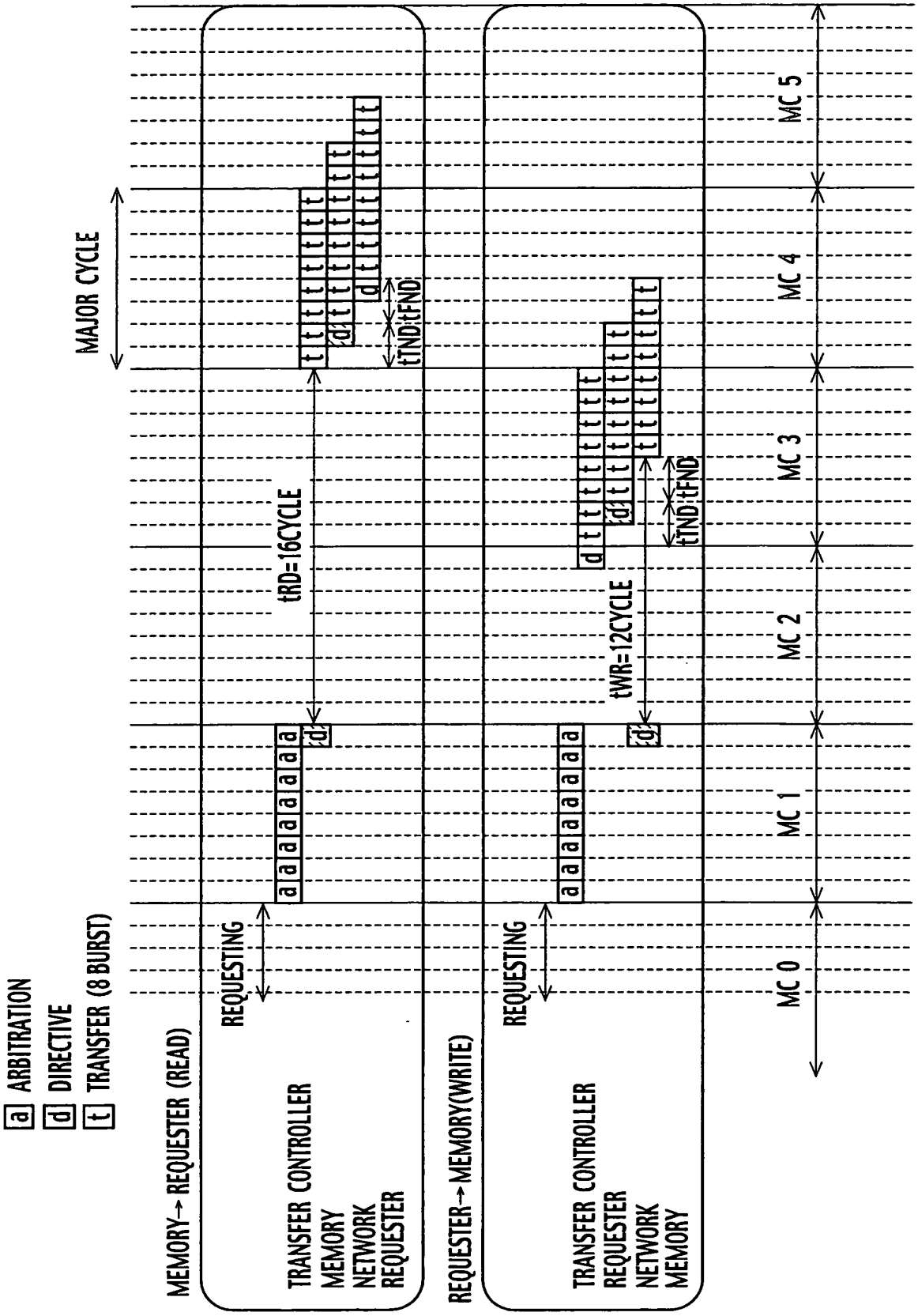

[a] ARBITRATION
[d] DIRECTIVE
[t] TRANSFER (8 BURST)
MEMORY→ REQUESTER (READ)
REQUESTING
TRANSFER CONTROLLER
MEMORY
NETWORK
REQUESTER
tRD=16CYCLE
REQUESTER→ MEMORY(WRITE)
REQUESTING
TRANSFER CONTROLLER
REQUESTER
NETWORK
MEMORY
tWR=12CYCLE
tTND:tFND
MAJOR CYCLE
MC 0
MC 1
MC 2
MC 3
MC 4
MC 5

FIG. 5

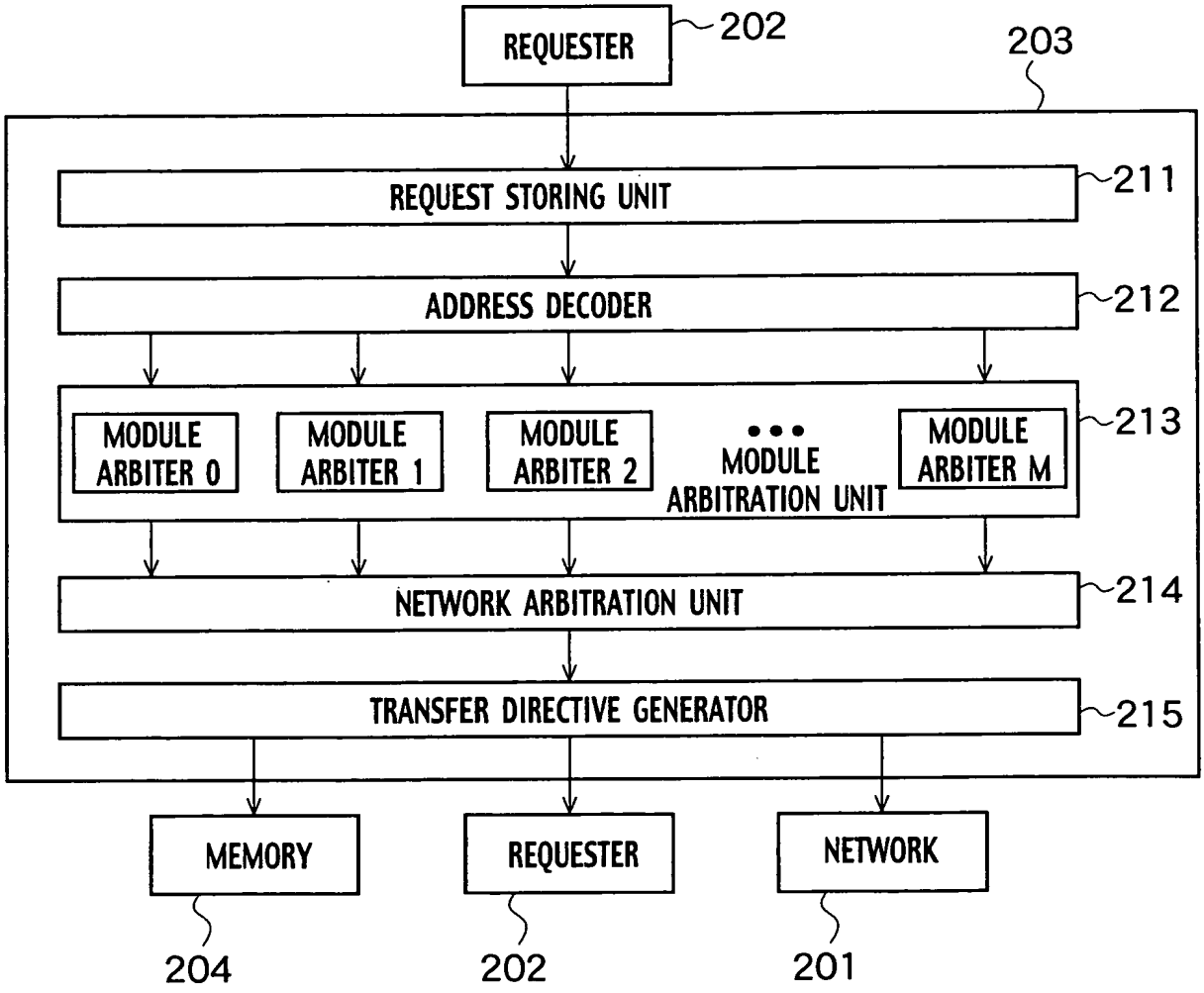

REQUESTER
202
203
REQUEST STORING UNIT
211
ADDRESS DECODER
212
MODULE ARBITER 0
MODULE ARBITER 1
MODULE ARBITER 2
MODULE ARBITER M
MODULE ARBITRATION UNIT
213
NETWORK ARBITRATION UNIT
214
TRANSFER DIRECTIVE GENERATOR
215
MEMORY
REQUESTER
NETWORK
204
202
201

FIG. 6A

REQID	MACRO #
0	3
1	0
2	1
3	0
4	2
5	3

FIG. 6B

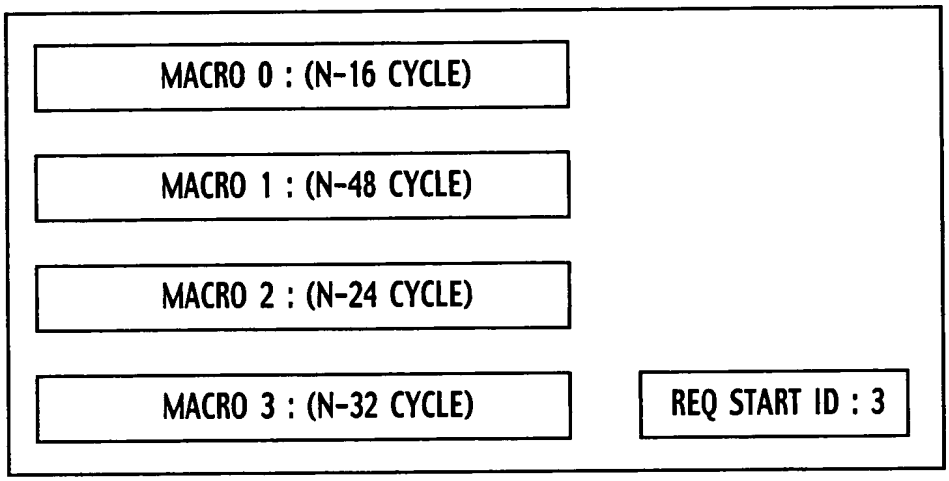


FIG. 7A

REQID	READ/WRITE
1	WRITE
2	READ
4	WRITE
5	WRITE
7	READ
8	READ
9	WRITE

FIG. 7B

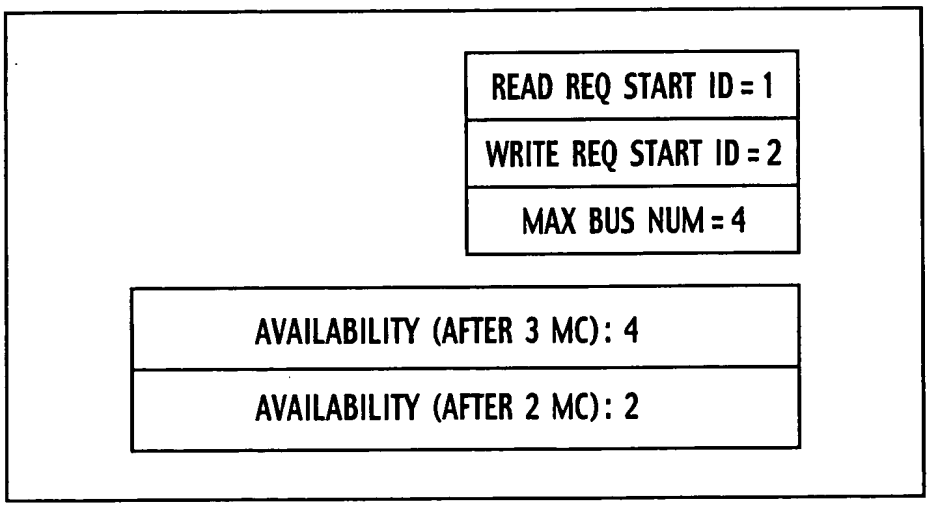


FIG. 8

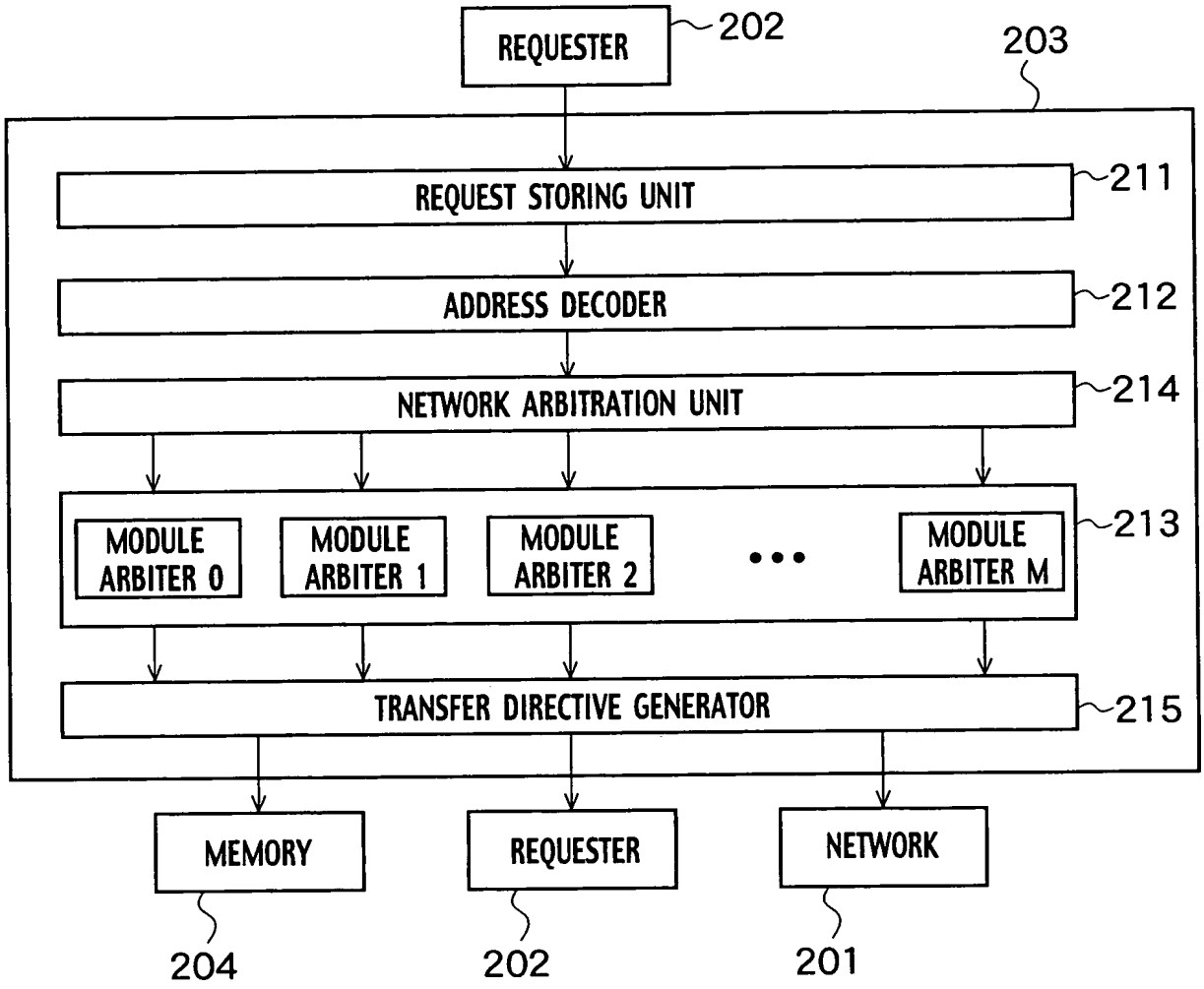

REQUESTER
202
203
REQUEST STORING UNIT
211
ADDRESS DECODER
212
NETWORK ARBITRATION UNIT
214
MODULE ARBITER 0
MODULE ARBITER 1
MODULE ARBITER 2
• • •
MODULE ARBITER M
213
TRANSFER DIRECTIVE GENERATOR
215
MEMORY
REQUESTER
NETWORK
204
202
201

FIG. 9

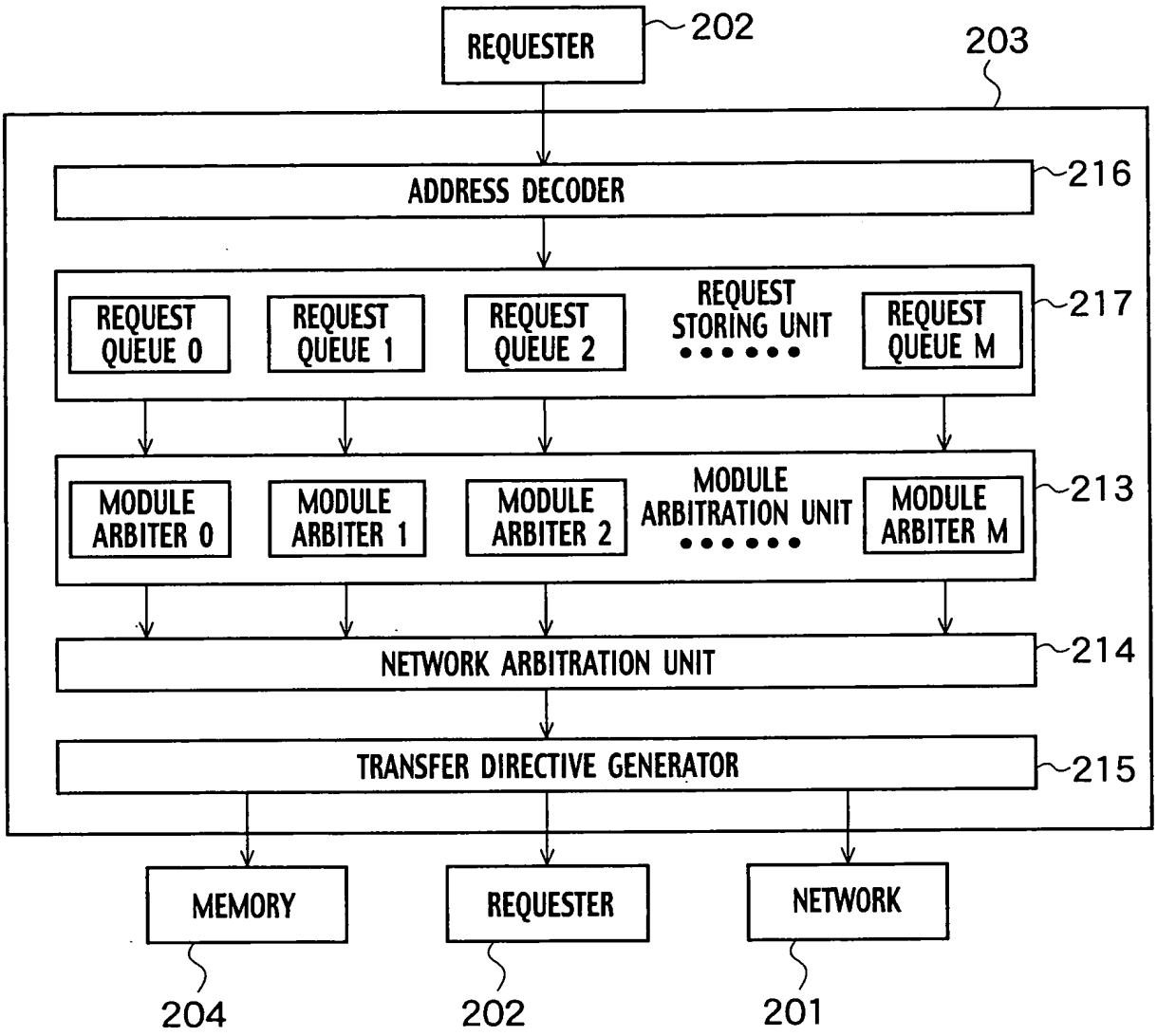

REQUESTER
202
203
ADDRESS DECODER
216
REQUEST QUEUE 0
REQUEST QUEUE 1
REQUEST QUEUE 2
REQUEST STORING UNIT
REQUEST QUEUE M
217
MODULE ARBITER 0
MODULE ARBITER 1
MODULE ARBITER 2
MODULE ARBITRATION UNIT
MODULE ARBITER M
213
NETWORK ARBITRATION UNIT
214
TRANSFER DIRECTIVE GENERATOR
215
MEMORY
REQUESTER
NETWORK
204
202
201

FIG. 10

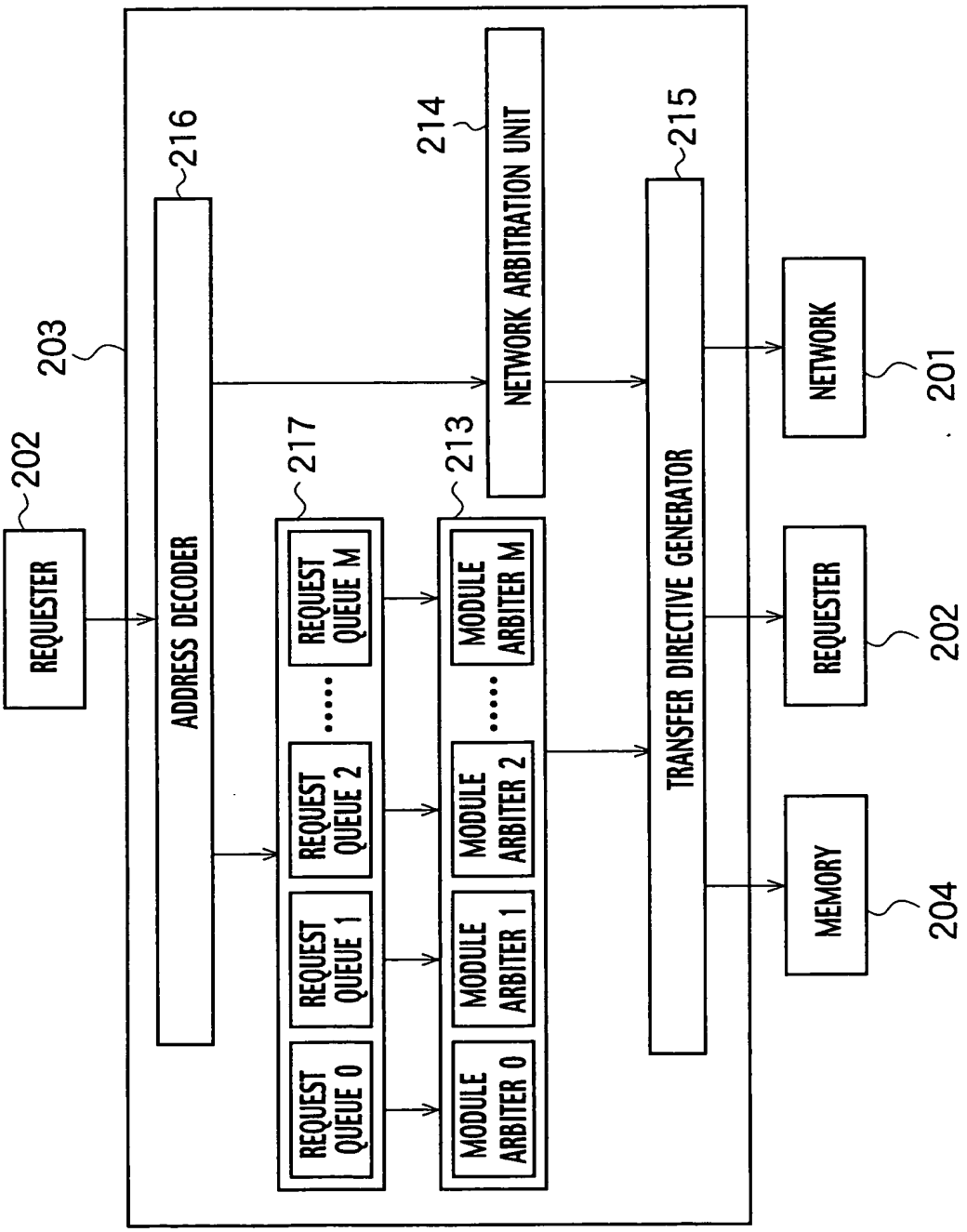

REQUESTER
202
203
ADDRESS DECODER
216
REQUEST QUEUE 0
REQUEST QUEUE 1
REQUEST QUEUE 2
REQUEST QUEUE M
217
MODULE ARBITER 0
MODULE ARBITER 1
MODULE ARBITER 2
MODULE ARBITER M
213
214
NETWORK ARBITRATION UNIT
215
TRANSFER DIRECTIVE GENERATOR
NETWORK
201
REQUESTER
202
MEMORY
204

FIG. 11

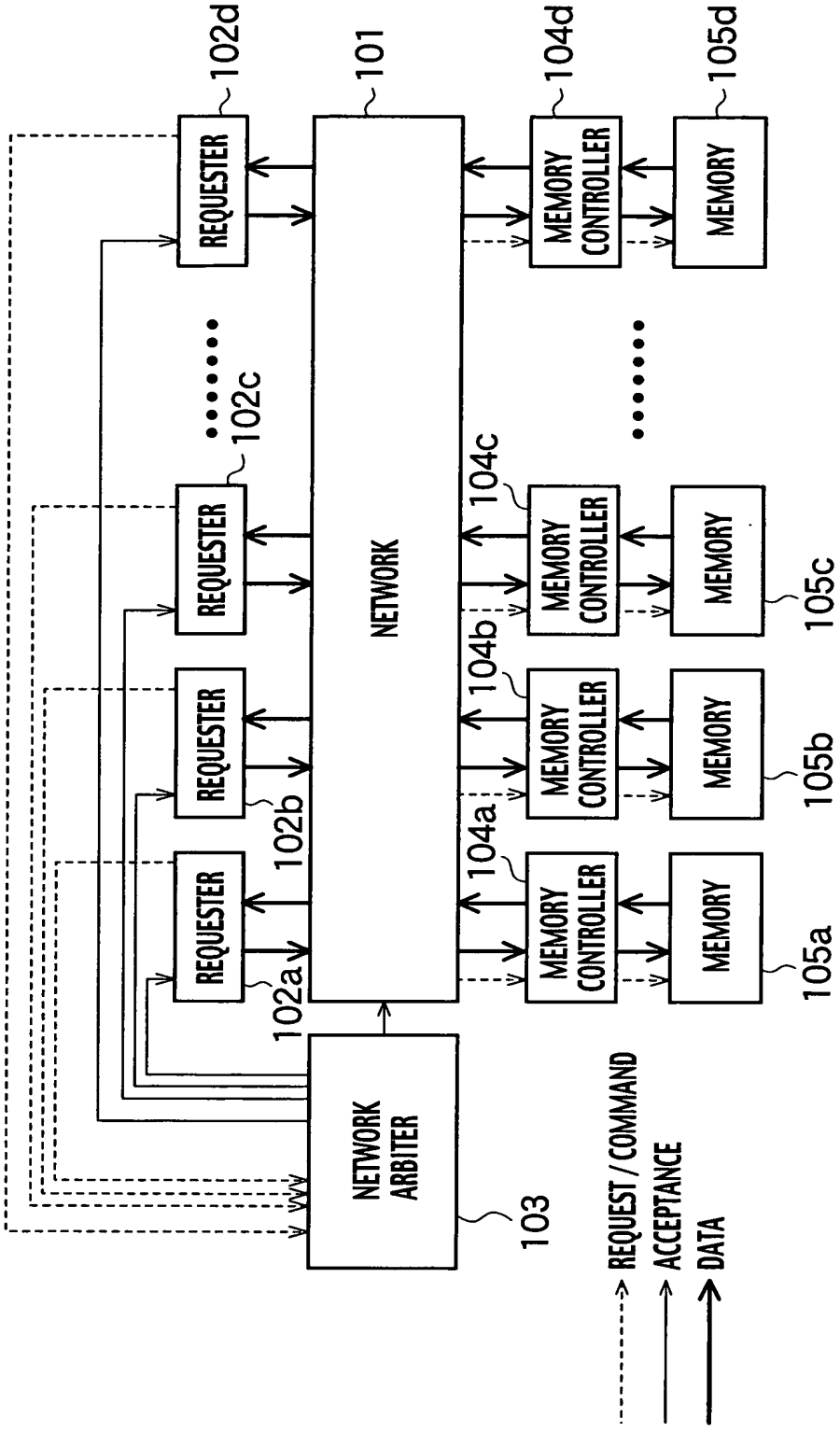
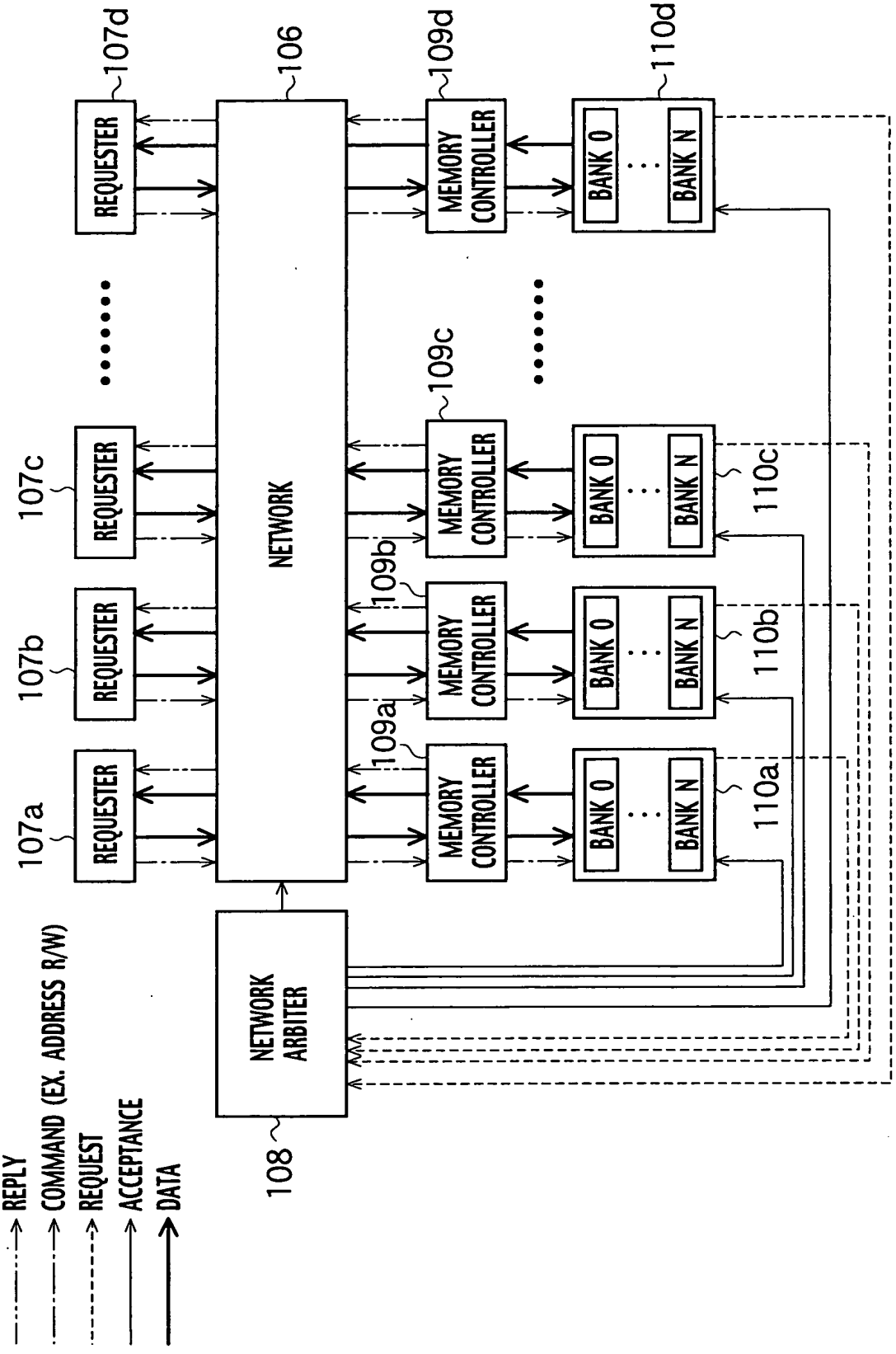

REQUESTER
102d
101
NETWORK
MEMORY CONTROLLER
104d
MEMORY
105d
102c
104c
105c
102b
104b
105b
102a
104a
105a
NETWORK ARBITER
103
REQUEST / COMMAND
ACCEPTANCE
DATA

FIG. 12


REQUESTER
107a
107b
107c
107d
NETWORK
106
NETWORK ARBITER
108
MEMORY CONTROLLER
109a
109b
109c
109d
BANK 0
BANK N
110a
110b
110c
110d
REPLY
COMMAND (EX. ADDRESS R/W)
REQUEST
ACCEPTANCE
DATA